REMARKS

The abstract, specification, and drawings have been amended to correct informalities. Claims 8, 9, and 17 rejected as unparticular. Applicant requests reconsideration. The claims 8, 9, and 17 have been accordingly amended. Claims 1 and 12 were rejected and unpatentable over Lim in view of Abaunza and in further view of Markarian. Claims 2, 4-6, 13 and 16 were rejected as unpatentable over Lim in view of Abaunza in Markarian in view of Levy. Claim 15 was rejected in view of Lim in view of Abaunza in view of Markarian in view of Durrant. Claim 14 was rejected in view of Abaunza in view Markarian in view of Schmidl. Claims 8, 9 and 17 were found otherwise allowable. Claims 7, 18, and 19 were objected to as depending of rejected based claims. Applicant requests reconsideration.

The specification was amended to recite that the even and odd timing signals are alternately processed by the loop filters. The specification teaches that "The mixers 52a and 52b respectively mix odd and even data with the gate sampled outputs of gate samplers 48a and 48b to respectively provide e_{2k+1} odd and e_{2k} even timing signals that drive a loop filter 53, that in turn, controls a voltage controlled oscillator 54 used for generating the t_n timing signal." and teaches that "The e_{2k} even and e_{2k+1} odd timing error signals drive a loop filter 97 that in turn controls a VCO 98 that generates the $e^{-j\hat{\theta}}$ phase adjustment signal 59.", in connection with the carrier phase synchronizer and the symbol time synchronizer, respectively. As it is understood that the timing signals are alternately signals, by virtue of the 2kN and (2k+1)N alternating

times, the loop filter would process them alternately. The alternate timing signals are alternately processed. The specification now makes clear that the alternate timing signals are alternately processed by the loop filters.

Applicant extends appreciation for the thorough examination. The examination rejects the two independent base claims 1 and 12 as unpatentable. The examination is in error and hence the follow on unpatentable rejections of the depending claims becomes moot. As to base claims 1 and 12, there was fundamental failure to appreciate the nature of "data aided demodulation" purpose and the parallel processing architecture necessary to accomplish this purpose. It is firstly observed that the present invention generates the timing error signal from the input data signal itself rather than from a comparison between a received carrier signal and a local carrier signal. It is secondly observed that in order to provide the timing error signal from the input data signal itself, cross coupled or parallel processing is needed.

The specification describes two preferred embodiments. The related embodiment is directed to carrier phase tracking as claimed in the related application, whereas the present embodiment is directed to symbol timing tracking in the present application, both embodiments are commonly characterized as data aided tracking reflected by respective cross-coupled or parallel architectures as respectively shown in Figures 2B and 1B. Firstly, Figure 2B shows the carrier phase synchronizer with the inputs to mixers 92a and 92b having cross-coupled parallel data timing inputs. Secondly,

Figure 1B shows the symbol time synchronizer having parallel timing paths as inputs to the mixers 52a and 52b. Both embodiments have parallel timing signals originating from transforms d(t) 86 and 88, and 46a and 46b, that provide data aided clock signals that are effectively data signals, and hence, the timing synchronizers are data aided timing synchronizers.

Claim 1 and 12 recites inphase and quadrature serial data demodulators having filtering d(t) functions for generating odd and even filter responses in parallel that are then converted 50a and 50b into data used to form the estimate of the input data sequence. In parallel to these paths are the inphase and quadrature error magnitude generator for generating error magnitude signals. The mixers 46a and 46b operating upon both the data and error magnitude signals are for generating the timing error signal by the loop filter 53. As such, the loop filter 53 timing error is derived in part from the odd and even data signals, and hence, the timing error signal generation is data aided.

This is in contrast to the primary reference Lim, and particularly the phase error generator 117, including the respective I and Q phase error generators 118 and 119, respectively, as shown in Figure 8. As shown, there is no cross coupling between the error generators 118 and 119. The error generator 118 is further shown in detail in Figure 13, showing an expanded filter arrangement using a fix frequency input of 10.76MHz. This fixed frequency signal is used for coherent error phase detection between the input pilot tone and a local oscillator

for providing local coherent phase error signal generation, as is well known in the art. The system of Lim does not include data aid timing error generation, nor is any such capability discussed or even remotely suggested.

Abaunza is cited for generating odd and even data samples. As shown in Abaunza, the odd and even data signals are fed into a Synch Phase Reversal Detector 13 for monitoring the FIR filter output to determine whether the sync phase reversal signal has been transmitted within a predetermined window or time period. (Col 6 line 10) As such, Abaunza does not teach data aided timing error generation. Further, there is no known way how Lima and Abaunza could be possibly combined along the lines of their respective teachings directed to different purposes and different architectures. Lim in view Abaunza does not teach nor suggest data aided error timing generation using parallel architectures for coupling data signals into an error-timing generator. Allowance of the claims is respectfully requested.

Respectfully Submitted

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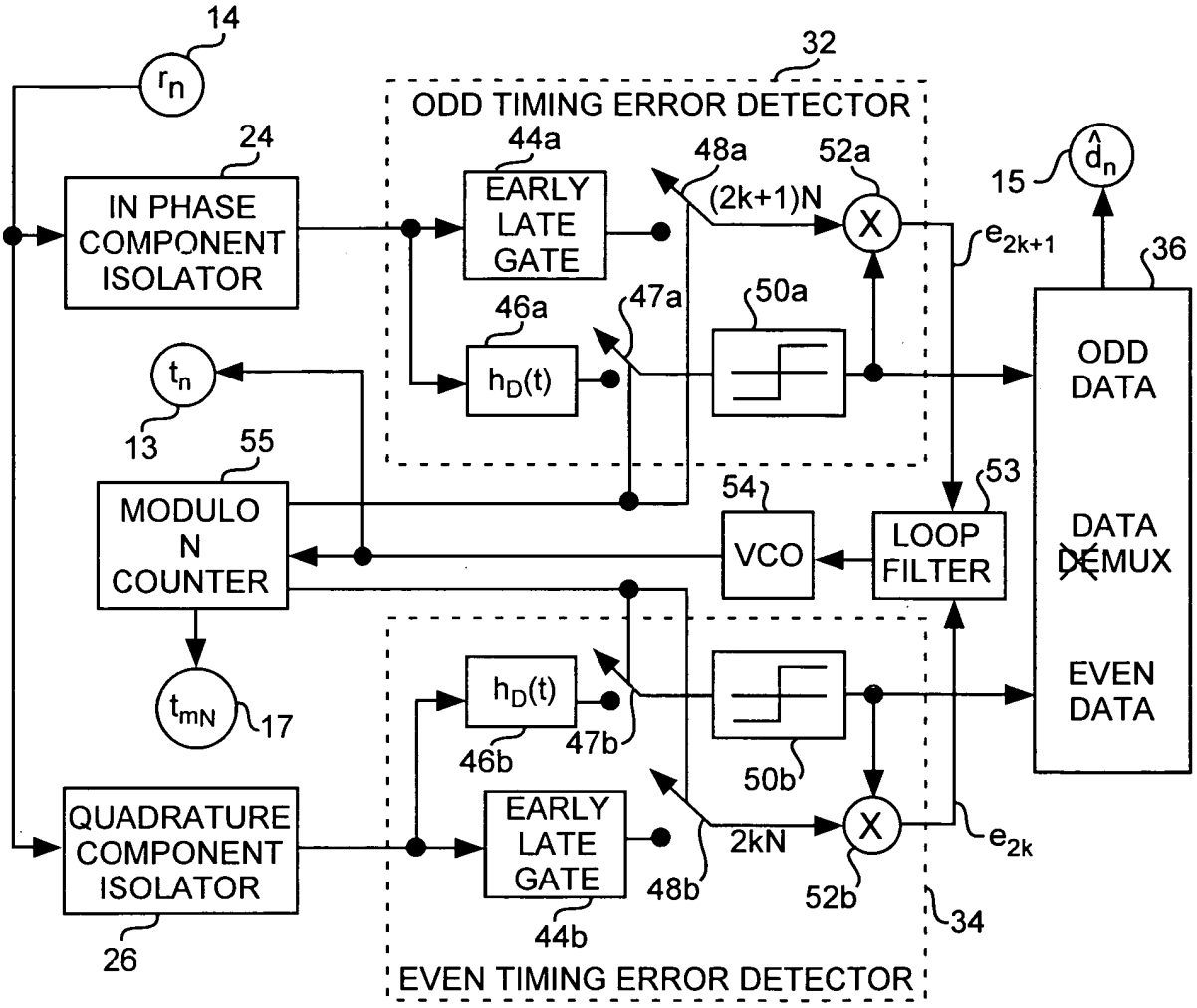
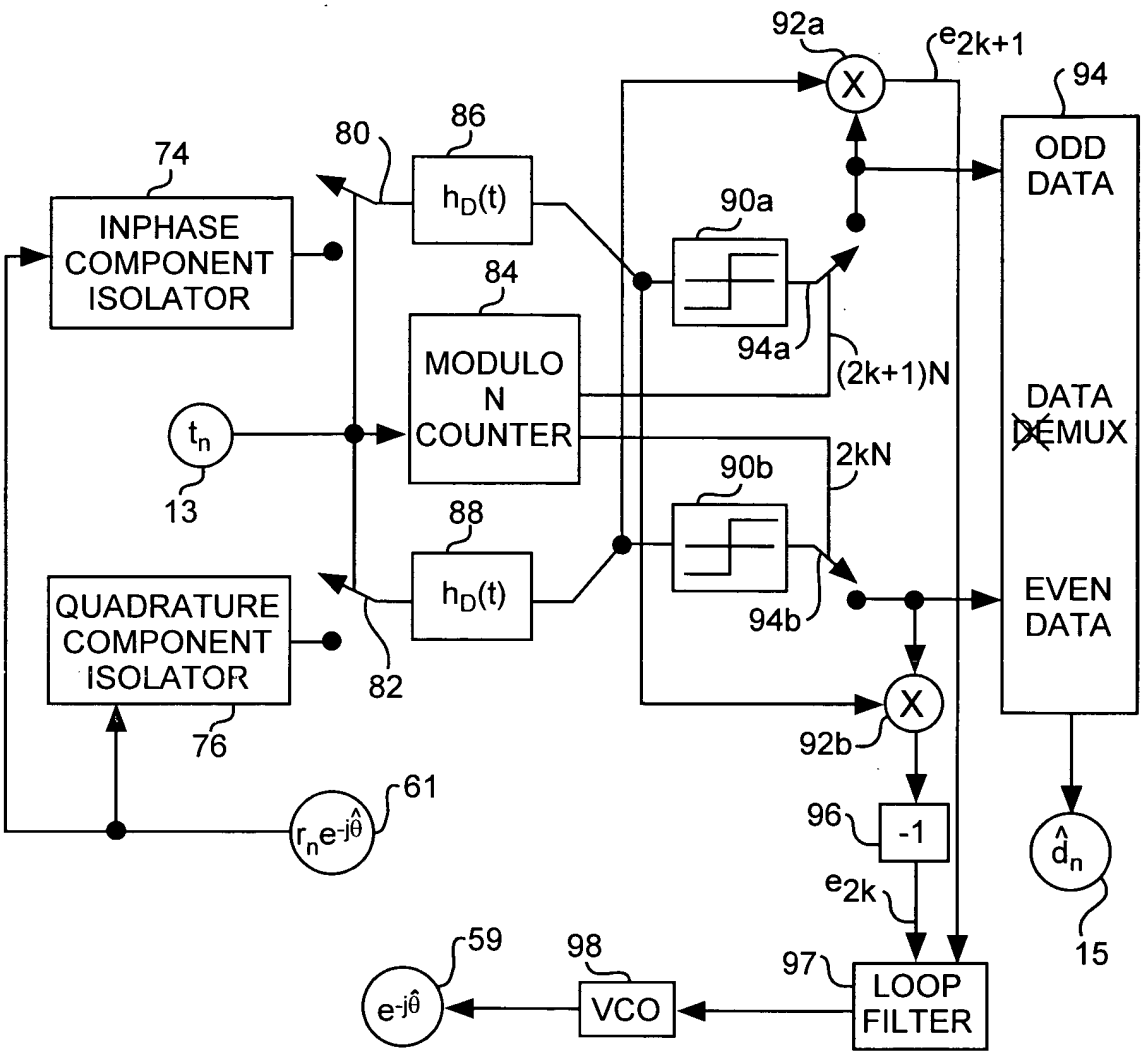
Annotated Sheet Showing Changes



SYMBOL TIME SYNCHRONIZER

FIG. 1B

Annotated Sheet Showing Changes



CARRIER PHASE SYNCHRONIZER

FIG. 2B